REMARKS

The above listing of claims is presented in accordance with the requests of the United States Patent and Trademark Office as expressed in a telephonic conference between the Examiner and Applicant's undersigned attorney on September 14, 2004.

Claims 1 through 13, 16, 19, 22, 25 through 27 and 29 through 31 are currently pending. No substantive changes have been made to the language of the pending claims (as compared to the Amendments mailed on August 9, 2001 and March 19, 2004) outside of formatting the claims in the requested manner.

Claim 3

Applicant notes that the Examiner has requested paragraph "e" of claim 3 to be underlined as though it was amended as compared U.S. Patent 5,348,164. However, Applicant submits that claim 3 has not been amended during prosecution of this reissue application and that it reads the same as set forth in U.S. Patent 5,348,164. As such, Applicant submits that paragraph "e" does not require underlining.

Support for Amendments to Claims

The Examiner has requested that an explanation of the support in the disclosure be set forth for all changes to the claims.

With respect to claim 5, the article "a" was placed before the term "first track" in the preamble (line 2) to correct a textual error. Additionally, the language associated with the positioning apparatus has been amended to remove the "capable of" language (lines 4 and 5 of claim 5) such that claim 5 affirmatively recites the positioning apparatus as having a first position and a second position. Support for this change may be found, for example, in the disclosure of U.S. Patent 5,348,164 at col. 2, lines 57-61 and in FIGS. 2-4, which states that, after receipt of an IC device, "station 18 will move downward and insert IC 15 into testing socket."

New claims 7 through 9 are directed to an integrated circuit testing apparatus which generally includes a receiving apparatus, a testing apparatus and a separating apparatus (and various limitations associated with such elements). Support for these claims may be found, for example, in the disclosure of U.S. Patent 5,348,164 at column 2, line 51 through col. 3, line10

and in FIGS. 2-4. The cited passage includes the following explanation of the claimed subject matter:

> Referring to FIG. 2 ...[t]he IC will slide into testing station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 2, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30 ... After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

New claims 10 through 12 are directed to an integrated circuit testing apparatus which generally includes a loading apparatus, a receiving apparatus, a testing apparatus and a separating apparatus (and various limitations associated with such elements). Support for these claims may be found, for example, in the disclosure of U.S. Patent 5,348,164 at column 2, line 51 through col. 3, line10 and in FIGS. 2-4. The cited passage includes the following explanation of the claimed subject matter:

> Referring to FIG. 2, there is a sectional side view of the IC testing device 11 comprising the following elements: There is a portion of a singulation station's bottom table 44, where an IC 15 has slid down onto loading ramp or track 16. The IC will slide into testing station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 2,

insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30 ... After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

Each of claims 13, 16, 19, 22, 27 and 31 are directed to methods of testing an integrated circuit which generally include various acts of handling the integrated circuit, testing the integrated circuit to determine whether it is defective or nondefective, and specified acts of handling the integrated circuit depending on whether it has been determined to be defective or nondefective. Support for these claims may be found, for example, in the disclosure of U.S. Patent 5,348,164 at column 2, line 51 through col. 3, line10 and in FIGS. 2-4. The cited passage includes the following explanation of the claimed subject matter:

Referring to FIG. 2, there is a sectional side view of the IC testing device 11 comprising the following elements: There is a portion of a singulation station's bottom table 44, where an IC 15 has slid down onto loading ramp or track 16. The IC will slide into testing station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 2, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30 ... After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed

to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

Claims 25 and 26 are directed to an apparatus for testing singulated integrated circuits. The apparatus generally includes a testing apparatus, a holding station, and a first and a second track to receive integrated circuits from the holding station (and various limitations associated with such elements). Support for these claims may be found, for example, in the disclosure of U.S. Patent 5,348,164 at column 2, line 51 through col. 3, line10 and in FIGS. 2-4. The cited passage includes the following explanation of the claimed subject matter:

> Referring to FIG. 2 ...[t]he IC will slide into testing station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 2, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30 ... After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

Claim 29 directed to an apparatus for testing singulated integrated circuits. The apparatus generally includes a loading apparatus, a testing apparatus, a holding station, and a first and a second track to receive integrated circuits from the holding station (and various limitations associated with such elements). Support for these claims may be found, for example, in the disclosure of U.S. Patent 5,348,164 at column 2, line 51 through col. 3, line10 and in FIGS. 2-4. The cited passage includes the following explanation of the claimed subject matter:

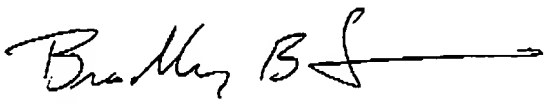
> Referring to FIG. 2, there is a sectional side view of the IC testing device 11 comprising the following elements: There is a portion of a singulation station's bottom table 44, where an IC 15 has slid down onto loading ramp or track 16. The IC will slide into testing station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 2, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30 ... After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for the next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

Applicant, therefore, respectfully submits that there is adequate support in the disclosure of U.S. Patent 5,348,164 for the changes to the claims herein as is explained hereinabove.

CONCLUSION

Applicant's undersigned attorney hereby authorizes the Examiner to enter the reformatted listing of claims set forth hereinabove as an Examiner's amendment. Applicant submits that the case is in condition for allowance and respectfully requests the same. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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